FEATURES

- Four Full-Duplex Lanes
- Data rate up to 10.3125 Gbps/lane
- Hot-Pluggable interface
- Low latency, low weight, and low power consumption
- Compliant with SFF-8436, SFF-8679, IEEE802.3ba
- EMI performance match FCC class B
- Storage, Network, Server, NIC, switch

Ordering Information

ELII-EBS0A0 – FXXXXXX

- 0A0=SR4
- S=Transceiver
- B=40G
- E=QSFP

OVERVIEW

ELII is a company which is devoted to providing reliable and outstanding optical modules. ELII QSFP 40G SR4 transceiver is a high-speed solution with cost-effective design.

1.1. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	Ts	-40	85	°C	
Supply Voltage	Vcc	-0.5	3.6	V	
Data Input Voltage (Single-Ended)		-0.5	Vcc+0.5	V	
Storage Relative Humidity	RH	5	85	%	
RX Optical Damage Threshold per lane	DT	3.4		dBm	

1.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Temperature	Tc	0	40	70	°C	
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Data Rate per lane			10.3125		Gbps	
Control Input Voltage High	Vih	2		Vcc+0.3	V	
Control Input Voltage Low	Vil	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate				400	KHz	
Receiver Differential Data Output Load	Z_d		100		Ohms	
Fiber Length (OM3)				300	m	
Fiber Length (OM4)				400	m	

1.3. Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Consumption	P			1.5	W	
Power Supply Current	Icc			450	mA	
TRx Power-On Initialization Time				2000	ms	Note 1
Data Input Differential Peak-to-Peak Voltage Swing	V_{DIFF}	200		1200	mVpp	
Data Output Differential Peak-to-Peak Voltage Swing		200		900	mVpp	Note 1

Note 1: AC-Coupled with 100Ω differential output impedance.

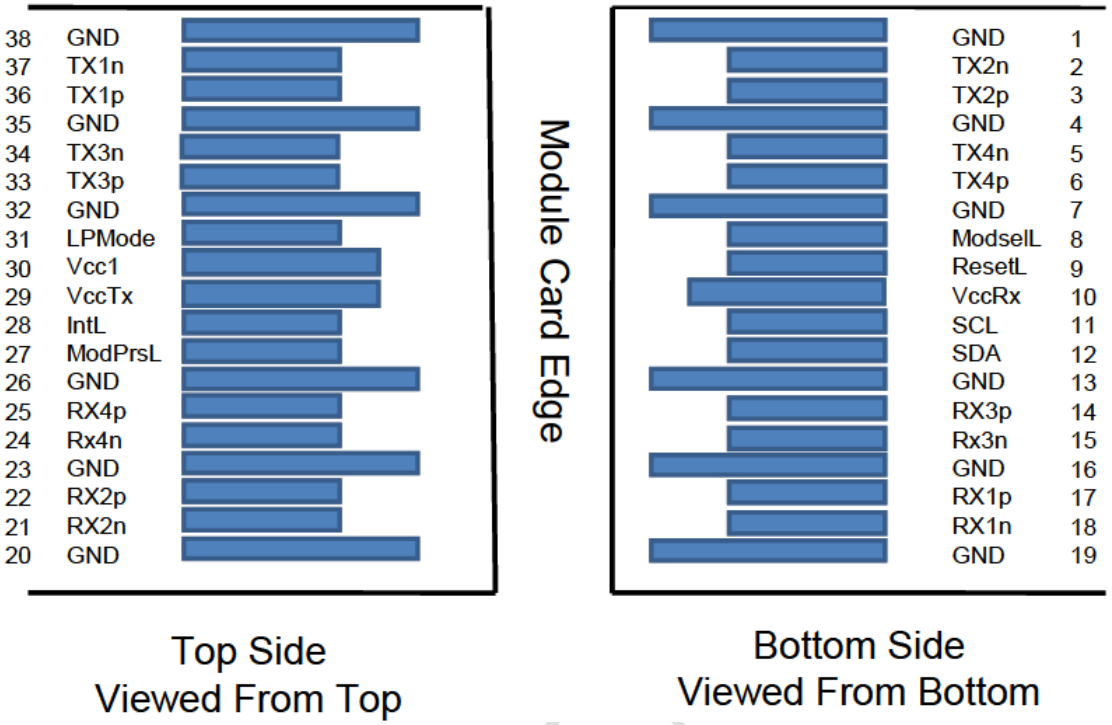
1.4. Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Central Wavelength	λ	840		860	nm	
Spectral Width – RMS	Δλ			0.65	nm	
Average Output Power, each lane	PO	-7.6		2.4	dBm	
Optical Extinction Ratio	ER	3			dB	
Disabled Output Optical Power	PO_OFF			-30	dBm	
Eye Mask Coordinates: X1, X2, X3; Y1, Y2, Y3.		Specification Value 0.23, 0.34, 0.43; 0.27, 0.35, 0.4			UI	Note 1
Receiver						
Central wavelength, each lane	λ	840	850	860	nm	
Damage Threshold		3.4			dBm	
Receiver Sensitivity, each lane	P_{IN}	-9.5		2.4	dBm	Note 2
LOS Assert	P_A	-30			dBm	
LOS De-Assert	P_D			-9	dBm	
LOS Hysteresis		0.5			dB	

Note 1: Hit ratio= 5×10^{-5} per sample.

Note 2: Measured with 10.3125-Gbps of PRBS-31 at 10^{-12} BER.

1.5. Contact Description



1.6 Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

1.7 QSFP transceiver Mechanical Dimensions

Unit: mm